

LISTING OF THE CLAIMS

1-79. (Canceled).

80. (Currently amended) A method of operating an active pixel CMOS imager, comprising:

activating a first address circuit for a first pixel of a pixel array and a second address circuit for a second pixel adjacent to said first pixel, said first pixel and said second pixel being in a row of pixels, said first address circuit consisting of a first row select line and a shared column line, and said second address circuit consisting of a second row select line and said shared column line;

~~activating a first pixel in a row of pixels connected to a shared column line using a at least one of the first row select line and then subsequently activating an adjacent second pixel in the row of pixels connected to the shared column line using a the second select row select line, wherein the first row select line and the second row select line each run along the row of pixels and are not connected to pixels of any other row of the array, the first and second pixels disposed in a pixel array;~~

~~resetting a voltage level of a node to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array;~~

~~transferring charge collected by the first pixel to the node;~~

~~detecting the charge at the node; and~~

~~generating an output signal over the shared column line corresponding to [[the]] charge detected at the node accumulated by at least one of the first pixel and second pixel.~~

81. (Previously Presented) The method of claim 80, wherein the shared column line extends approximately linearly across the pixel array.

82. (Previously presented) The method of claim 81, wherein the first and second row select lines extend approximately linearly across the pixel array.

83. (Previously presented) The method of claim 80, wherein the first and second row select lines extend approximately linearly across the pixel array.

84. (Currently amended) A method of operating a system, comprising:

focusing an image on an active pixel CMOS imager, the imager comprising a pixel array;

activating a first address circuit for a first pixel of a pixel array and a second address circuit for a second pixel adjacent to said first pixel, said first pixel and said second pixel being in a row of pixels, said first address circuit consisting of a first row select line and a shared column line, and said second address circuit consisting of a second row select line and said shared column line;

~~activating a addressing the first pixel in a row connected to a shared column line using [[a]] the first row select line and then subsequently ~~activating an adjacent~~ addressing the second pixel in the row connected to the shared column line using [[a]] the second row select line, the pixel array comprising the first and second pixels and the first row select line and second row select line each running along the length of the row and not being connected to pixels of any other row;~~

resetting a voltage level of a node associated with the first pixel to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array;

transferring charge collected by the first pixel to the node;

detecting the charge at the node; and

generating an output signal over the shared column line, the output signal corresponding to the image.

85. (Previously Presented) The method of claim 84, wherein the shared column line extends approximately linearly across the pixel array.

86. (Previously presented) The method of claim 85, wherein the first and second row select lines extend approximately linearly across the pixel array.

87. (Previously presented) The method of claim 84, wherein the first and second row select lines extend approximately linearly across the pixel array.

88. (Currently amended) An active pixel CMOS imager, comprising:

a plurality of pixels to generate an output signal associated with detected light, the plurality of pixels arranged in rows and columns of an array, each said row having both odd and even pixels, wherein each said odd pixel is addressed by a respective first address circuit consisting essentially of an odd row select line and a shared column line, and wherein each said even pixel is addressed by a respective second address circuit consisting essentially of an even row select line and a shared column line, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels;

a plurality of column lines comprising the column lines of the first address circuit and the second address circuit, each of the plurality of column lines being connected to at least two adjacent pixels of a row in the array, the column lines being connected to output circuitry to output the signal;

~~a plurality of odd row select lines orthogonal to the column lines to address odd pixels in the rows;~~

~~a plurality of even row select lines orthogonal to the column lines to address even pixels in the rows, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels;~~

a column driver to address pixels connected to the column lines; and

a row driver to address pixels through the odd row select lines and the even row select lines.

89. (Previously Presented) The imager of claim 88, wherein the column lines extend approximately linearly across the array.

90. (Previously Presented) The imager of claim 89, wherein the odd and even row select lines extend approximately linearly across the array.

91. (Previously Presented) The imager of claim 88, wherein the odd and even row select lines extend approximately linearly across the array.

92. (Previously Presented) The imager of claim 88, further comprising a plurality of reset lines that extend approximately linearly across the array.

93. (Currently amended) A method of operating a CMOS imager, comprising:

providing a first address circuit for even pixels of row of pixels and a second address circuit for odd pixels of the row of pixels, said first address circuit consisting essentially of an even row select line and a plurality of shared column lines, and said second address circuit consisting essentially of an odd row select line and said plurality of shared column lines, wherein the even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels;

addressing the even pixels in a row of pixels of an array of pixels using a row driver coupled to ~~[[an]]~~ the even row select line;

providing a first output signal associated with light detected by the even pixels to ~~[[a]]~~ the plurality of shared column lines coupled to the even pixels;

addressing the odd pixels in the row of pixels via an odd row select line, wherein the ~~even row select lines do not address the odd pixels and the odd row select lines do not address the even pixels~~ using the row driver coupled to the odd row select line; and

providing a second output signal associated with light detected by the odd pixels to the plurality of shared column lines ~~coupled to the odd pixels~~.

94. (Previously Presented) The method of claim 93, wherein the column lines extend approximately linearly across the array and are approximately orthogonal to both the even row select line and the odd row select line.

95. (Previously Presented) The method of claim 94, wherein the odd and even row select lines extend approximately linearly across the array.

96. (Previously Presented) The method of claim 94, further comprising a plurality of reset lines that extend approximately linearly across the array.

97. (Currently amended) An imaging device, comprising:

a row comprising a first pixel and a second pixel;

the first and second pixels being joined by a diagonal active area component;

a first even row line connected with the first pixel;

a second odd row line connected with the second pixel, wherein said first even row line and said second odd row line are associated with said row and not any other row; [[and]]

a column line connected with the first and second pixels at the diagonal active area component;

a first address circuit for the first pixel consisting essentially of the first even row select line and a shared column line; and

a second address circuit for the second pixel consisting essentially of the second odd row select line and said shared column line, wherein the first even row select line does not address the second pixel and the second odd row select line does not address the first pixel.

98. (Previously Presented) The imaging device of claim 97, wherein the row further comprises a plurality of first pixels and a plurality of second pixels.

99. (Previously presented) The imaging device of claim 97, wherein the first even row line and second odd row line each extends substantially linearly across an array of pixels.

100. (Previously Presented) The imaging device of claim 97, further comprising a first reset line for the first pixel and a second reset line for the second pixel.

101. (Previously presented) The imaging device of claim 100, wherein each of the first even row line, second odd row line, first reset line, and second reset line extends substantially linearly across the first and second pixels.

102. (Currently amended) An imaging device, comprising:

a pixel array comprising a row ~~comprising a plurality~~ of first pixels and a ~~plurality of~~ second pixels;

~~a first row address line connected with the first pixels;~~

~~a second row address line connected with the second pixels, wherein the second row address line is not connected with the first pixels and the first row address line is not connected with the second pixels;~~

~~a respective column line for each pair of first and second pixels of the row a first address circuit for the first pixels consisting essentially of a first row select line and a plurality of shared column lines;~~

~~a second address circuit for the second pixels consisting essentially of a second row select line and said plurality of shared column lines, wherein the first row select lines do not address the second pixels and the second row select lines do not address the first pixels, each of the shared column lines being associated with a first pixel and a second pixel; and~~

~~a reset line connected to the plurality of first pixels.~~

103. (Previously Presented) The imaging device of claim 102, wherein the plurality of first pixels are every other pixel in the row.

104. (Previously Presented) The imaging device of claim 102, wherein each pair of first and second pixels of the row are arranged with the first and second pixels positioned adjacent each other along the column line.

105. (Previously Presented) The imaging device of claim 102, wherein each pair of first and second pixels are connected by a substantially diagonal active area.

106. (Currently amended) An imaging device comprising:

a row of pixels comprising a first plurality of pixels and a second plurality of pixels[[,]];

a first address ~~line-addressing-only~~ circuit for the first plurality of said pixels and a second address ~~line-addressing-only~~ circuit for the second plurality of said pixels, said first address circuit consisting essentially of a first row select line and a plurality of shared column lines, and said second address circuit consisting essentially of a second row select line and said plurality of shared column lines, wherein the first row select lines do not address the second plurality of pixels and the second row select lines do not address the first plurality of pixels[[;]] ~~a plurality of read-out lines,~~ each of said ~~read-out lines~~ plurality of shared column lines being connected to a first pixel of the first plurality of pixels and a second pixel of the second plurality of pixels; and

a reset line connected to at least the first plurality of pixels or the second plurality of pixels.